**Basic Electrical Science Lab  
Course Code: EE152**

**Laboratory Manual**

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Roll No: 20CSE1030

Section: B

Academic Session: April – August 2021

**National Institute of Technology Goa**



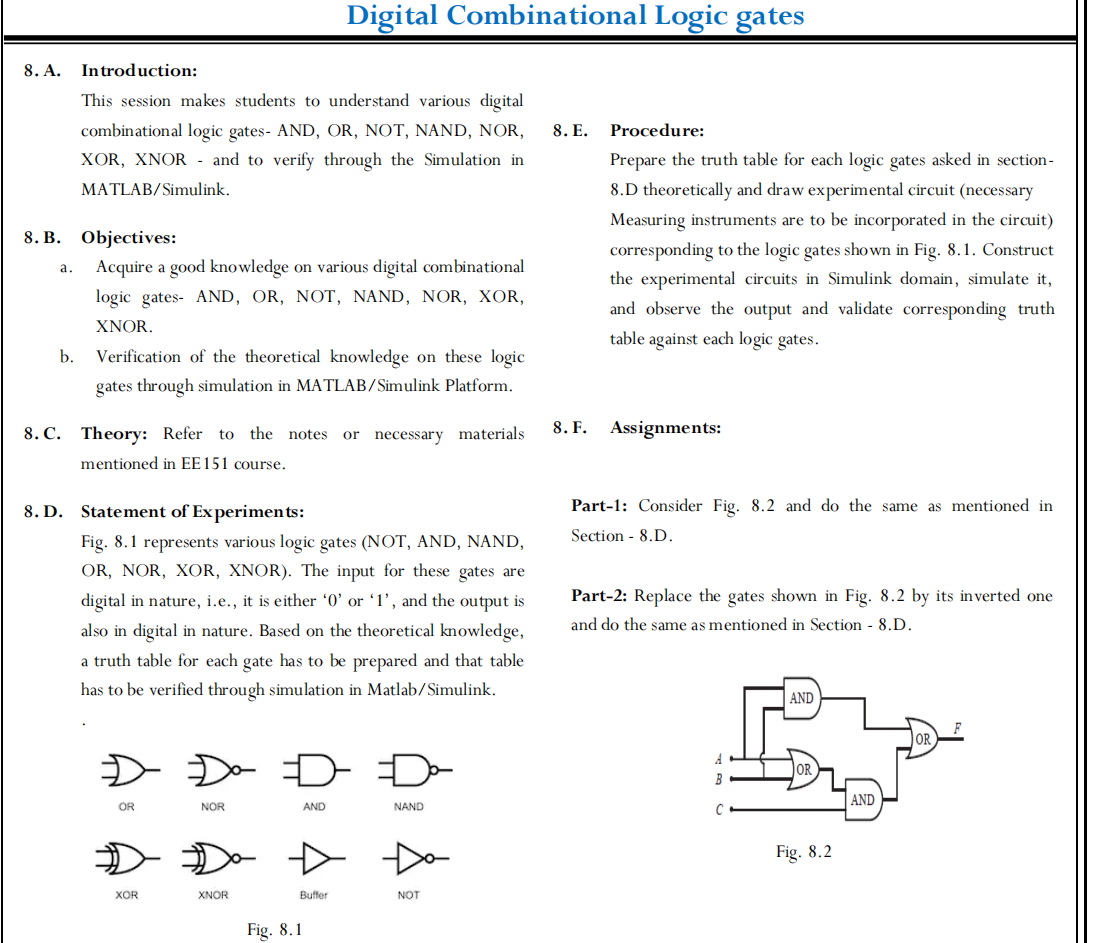
**CERTIFICATE**

This is to certify that Mr./ Ms. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ of Class B.Tech 1st year (2nd Sem), Division Sec A/B, bearing Roll. No.\_\_\_\_\_\_\_\_\_\_\_\_\_, has satisfactorily completed the course experiments in the Laboratory Course Basic Electrical Science Lab (EE152) in the academic year 2020-2021 in the Institution of National Institute of Technology Goa.

**Course Instructor**

**Table of Contents**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Sl. No.** | **Name of the Experiment** | **Pg. No.** | **Date of Experiment** | **Date of Submission** | **Marks/Expt.**  **(10 M)** |
| **1** | **Verification of Ohms Law** | **04** | **20-05-2021** | **23-05-2021** |  |
| **2** | **Verification of Kirchhoff's Laws – KVL and KCL** | **11** | **27-05-21** | **31-05-21** |  |
| **3** | **Verification of Thevenin’s and Norton’s Theorem** | **04** | **03-06-21** | **17-06-21** |  |
| **4** | **DC transient analysis of RC RL circuits** | **04** | **24-06-2021** | **02-07-21** |  |
| **5** | **Power analysis in AC circuits** | **04** | **1-07-2021** | **9-07-2021** |  |
| **6** | **Study of Diode Rectifier Circuits** | **05** | **8-7-2021** | **12-07-2021** |  |
| **7** | **Study of Digital Logic gates** | **05** | **15-07-2021** | **18-07-2021** |  |
| **8** | **Full-wave Diode Rectifier** |  |  |  |  |
| **9** | **Transient analysis of RL, RC and RLC Circuits** |  |  |  |  |
| **10** | **Digital Gate Circuits** |  |  |  |  |

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**Experiment 8**

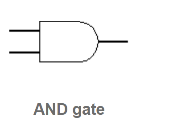
**Digital Combinational Logic Gates**

1. **Aim:** To verify the theoretical analysis of various digital combinational logic gates  
    NOT, AND, NAND, OR, NOR, XOR, XNOR
2. **Simulink Blockset used:** Logical operator AND, OR, NOR, NAND, NOT, XOR, XNOR. Display, scope, Pulse generator.
3. **Theory:**

* **Logic Gate:**

A logic gate is a device that acts as a building block for digital circuits. They perform basic logical functions that are fundamental to digital circuits. Most electronic devices we use today will have some form of logic gates in them. For example, logic gates can be used in technologies such as smartphones, tablets or within memory devices.

There are seven basic logic gates: AND, OR, XOR, NOT, NAND, NOR, and XNOR.

* AND Gate

The output is "true" when both inputs are "true." Otherwise, the output is "false."

* OR Gate

The output is "False" when both inputs are "false." Otherwise, the output is "true."



* NAND Gate

 The output is "false" if both inputs are "true." Otherwise, the output is "true." |

* XOR Gate

The output is "true" if inputs are different, and “false” when the inputs are same.

* NOT Gate

 If the input is "true", then the output is “false”. If the input is “false”, then the output is "true".

* XNOR Gate

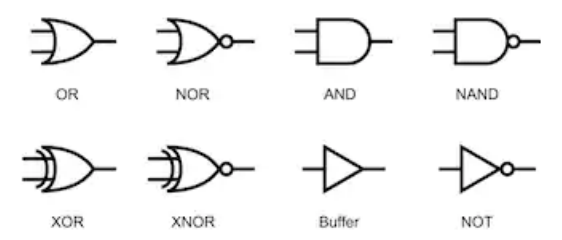
Its output is "true" if the inputs are the same, and "false" if the inputs are different.

* NOR Gate

 Its output is "true" if both inputs are "false." Otherwise, the output is "false."

1. **Statement of Experiments:**

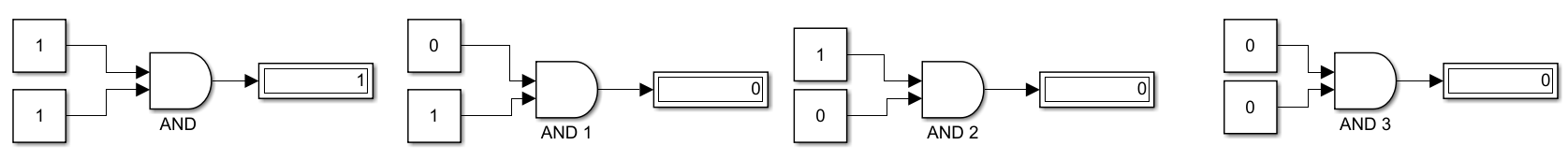
Fig. 8.1 represents various logic gates (NOT, AND, NAND, OR, NOR, XOR, XNOR). The input for these gates are digital in nature, i.e., it is either ‘0’ or ‘1’, and the output is also in digital in nature. Based on the theoretical knowledge, a truth table for each gate has to be prepared and that table has to be verified through simulation in MATLAB/Simulink.



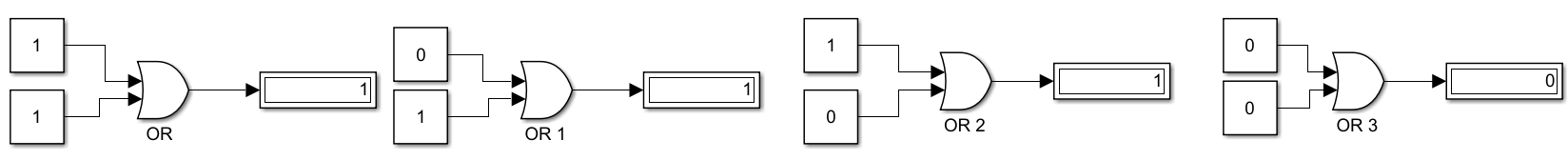
1. **Procedure:**

Prepare the truth table for each logic gates asked in Section-8.D theoretically and draw experimental circuit (necessary Measuring instruments are to be incorporated in the circuit) corresponding to the logic gates shown in Fig. 8.1. Construct the experimental circuits in Simulink domain, simulate it, and observe the output and validate corresponding truth table against each logic gates.

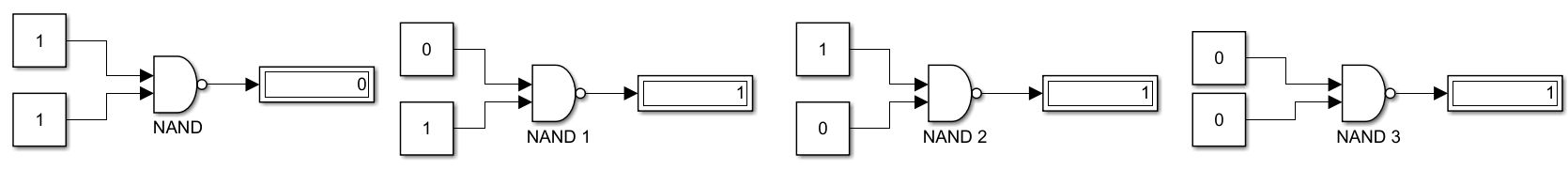
* Circuit Diagram:



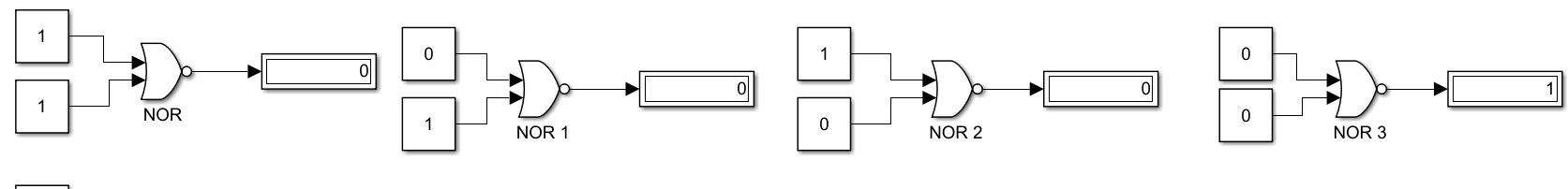
**Fig8a**: Input Output for AND gate



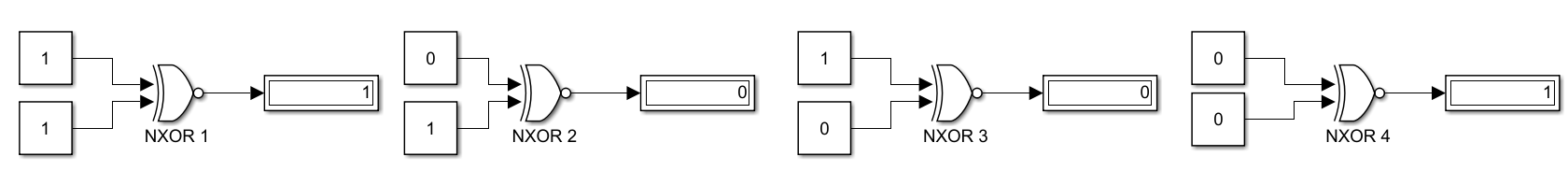
**Fig8b**: Input Output for OR gate



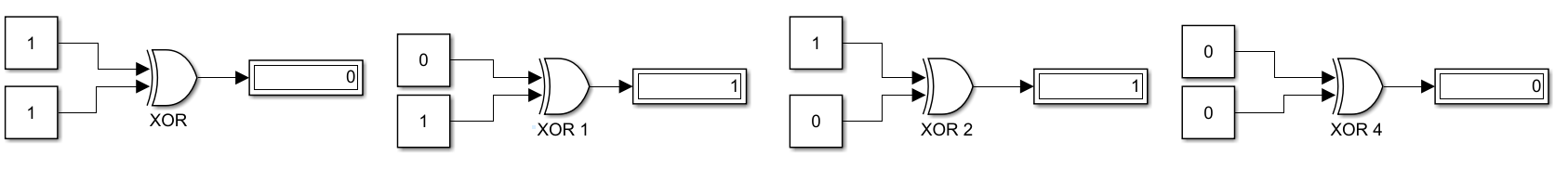
**Fig8c**: Input Output for NAND gate



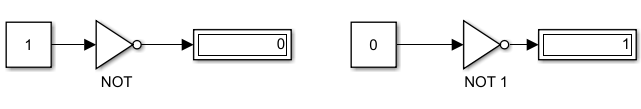
**Fig8d**: Input Output for NOR gate



**Fig8e**: Input Output for XNOR gate



**Fig8f**: Input Output for XOR gate



**Fig8g**: Input Output for NOT gate

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Logic Gate | Input | Input | Output | |
| Theoretical | Simulated |
| AND | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 |

**Table8a**: Comparison between theoretical and simulated outputs of AND Gate

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Logic Gate | Input | Input | Output | |
| Theoretical | Simulated |
| OR | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 |

**Table8b**: Comparison between theoretical and simulated outputs of OR Gate

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Logic Gate | Input | Input | Output | |
| Theoretical | Simulated |
| NAND | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 |

**Table8c**: Comparison between theoretical and simulated outputs of NAND Gate

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Logic Gate | Input | Input | Output | |
| Theoretical | Simulated |
| NOR | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 |

**Table8d**: Comparison between theoretical and simulated outputs of NOR Gate

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Logic Gate | Input | Input | Output | |
| Theoretical | Simulated |
| NXOR | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 |

**Table8e**: Comparison between theoretical and simulated outputs of XNOR Gate

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Logic Gate | Input | Input | Output | |
| Theoretical | Simulated |
| XOR | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 |

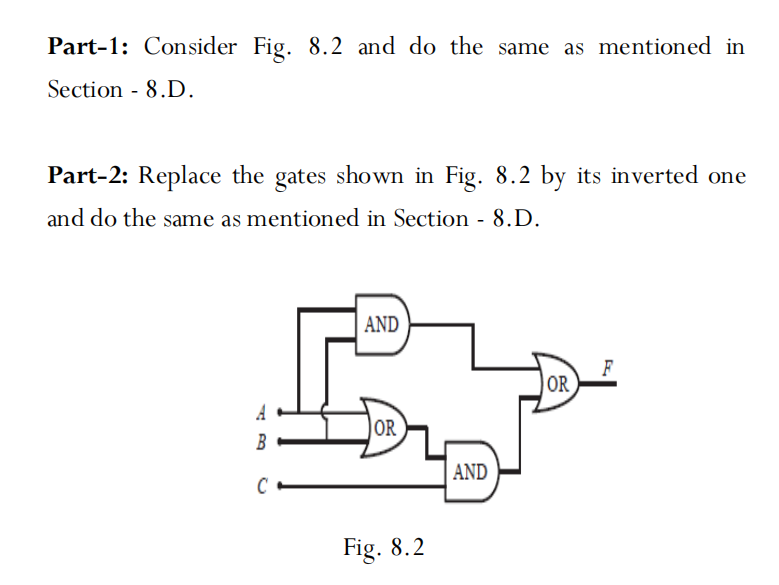
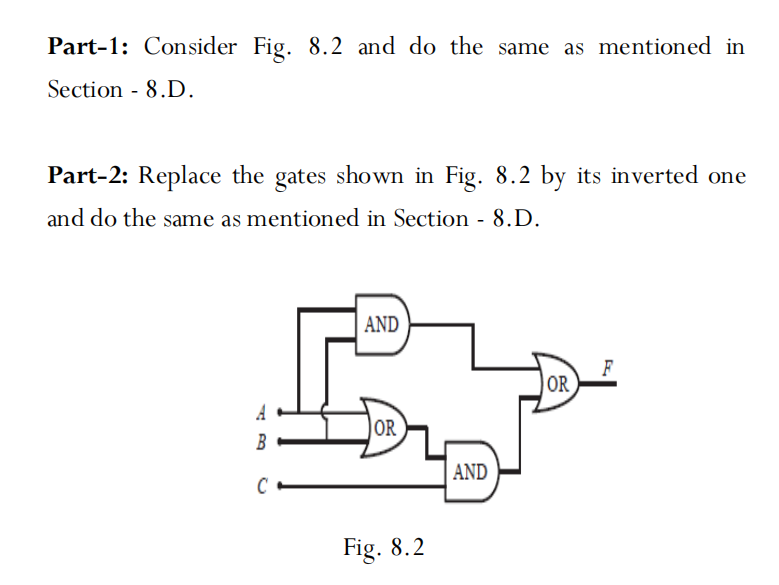
**Table8f**: Comparison between theoretical and simulated outputs of XOR Gate

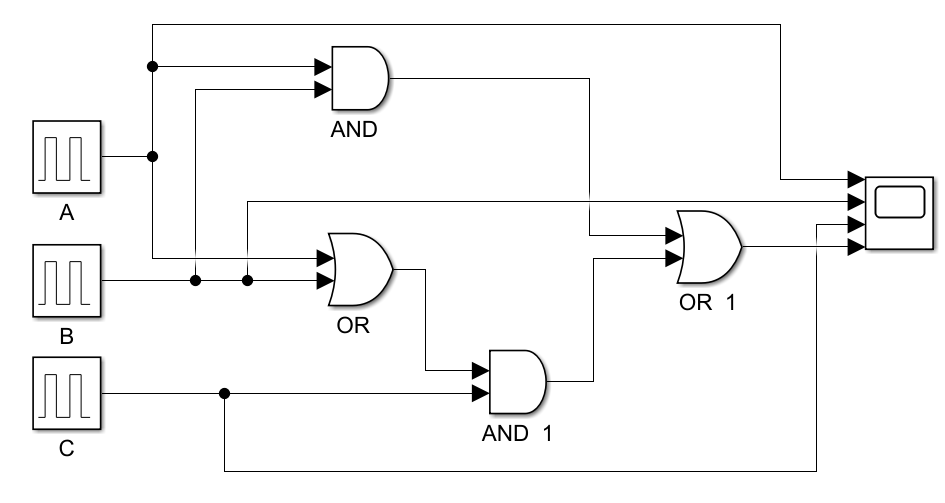
|  |  |  |  |
| --- | --- | --- | --- |
| Logic Gate | Input | Output | |
| Theoretical | Simulated |
| NOT | 1 | 0 | 0 |
| 0 | 1 | 1 |

**Table8g**: Comparison between theoretical and simulated outputs of NOT Gate

1. **Precautions:**
2. Ensure that ‘powergui’ block set is included in the Simulink file
3. Ensure that connections are properly made
4. Ensure that the scale of the graphs should be adjusted to the range in which the readings vary
5. **Conclusion:** Theoretical Knowledge on digital logic gates is verified through a Simulink platform.

Assignment:

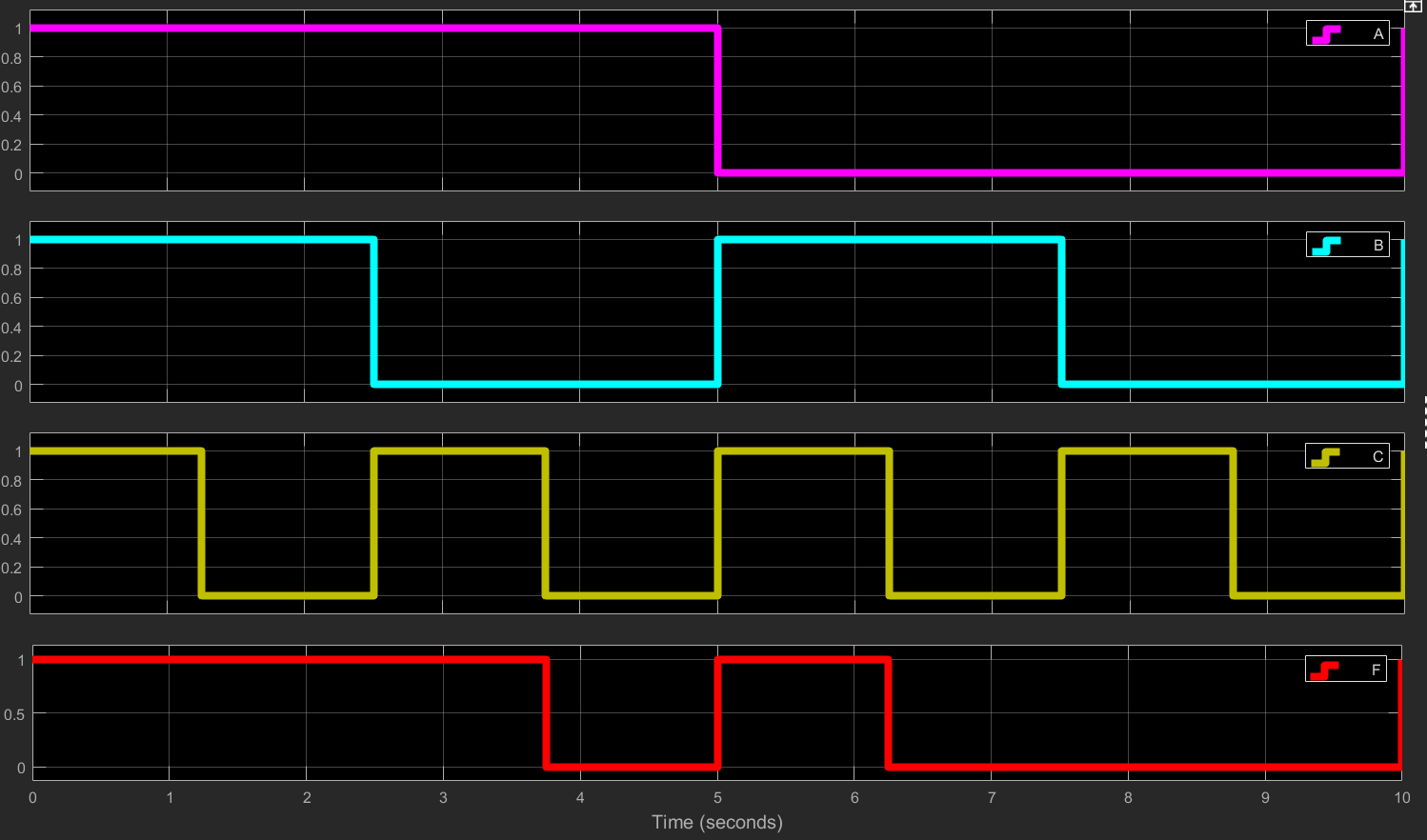




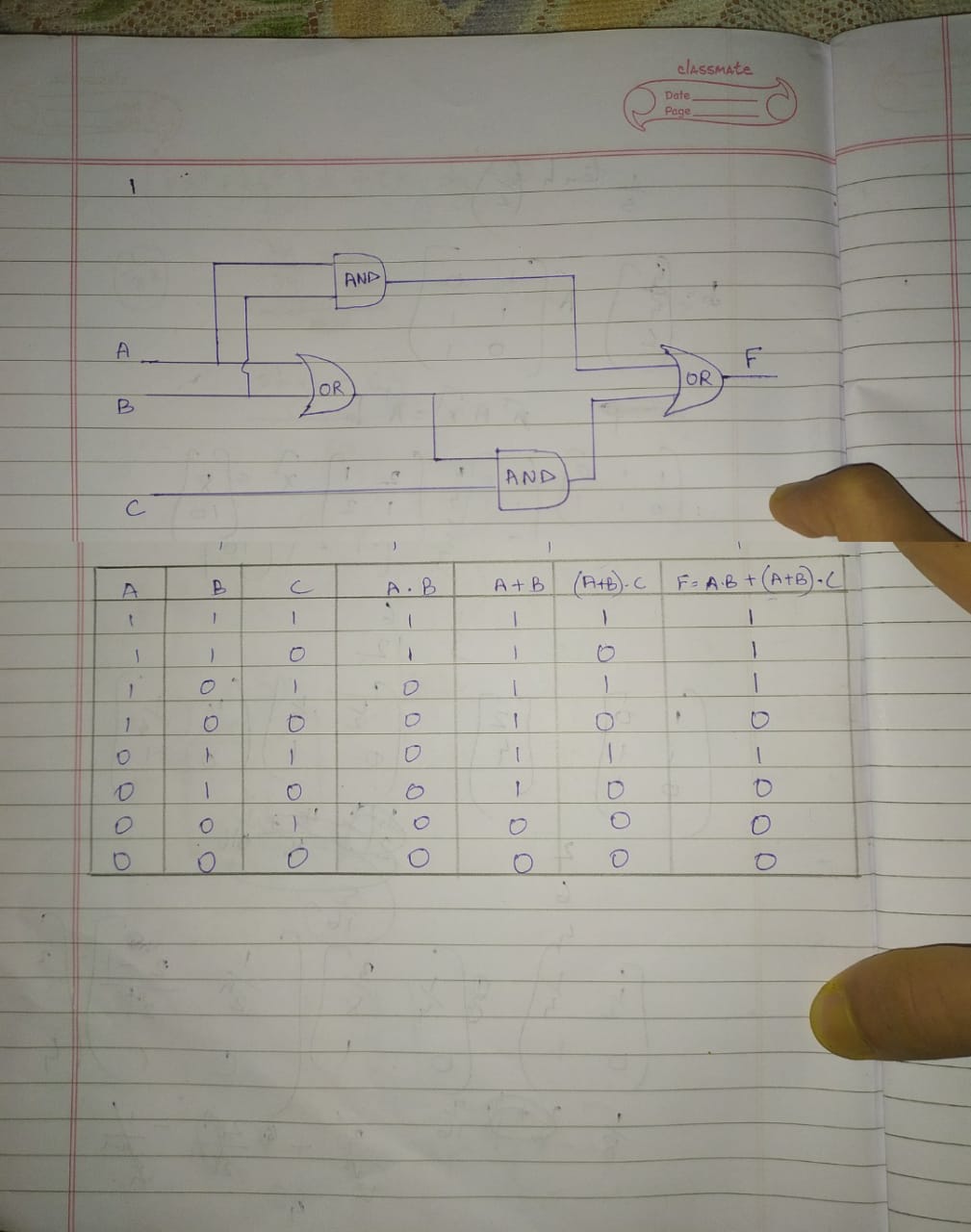
**Fig8h**: Simulink connections for circuit given in Fig 8.2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | Output F | |
| Theoretical | Simulated |
| 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 |

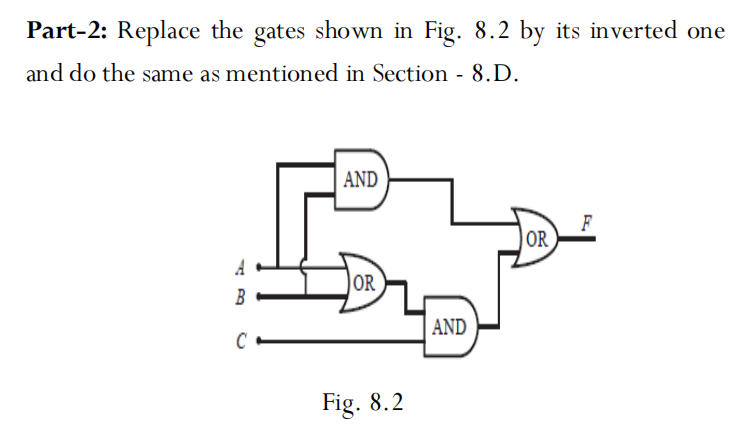
**Table8h**: Comparison between theoretical and simulated outputs of circuit in Fig

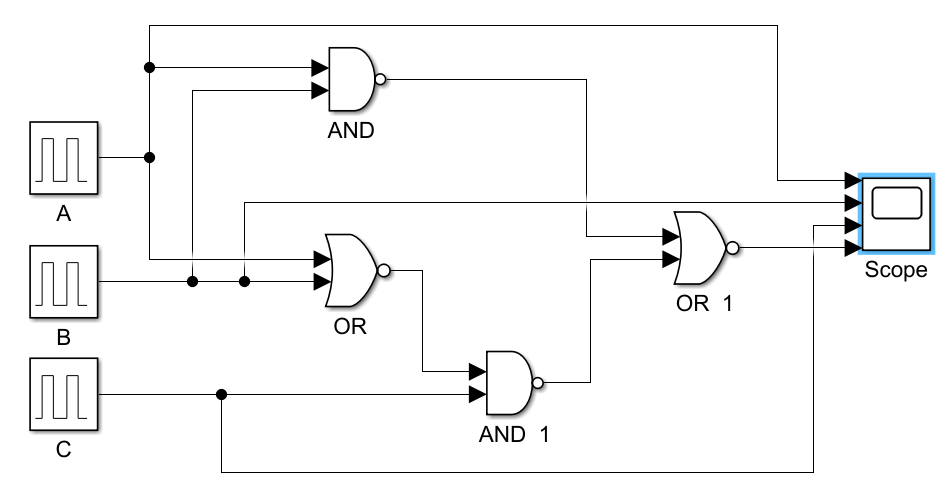
**Graphical Results;**

**Theoretical Results:**



Assignment:

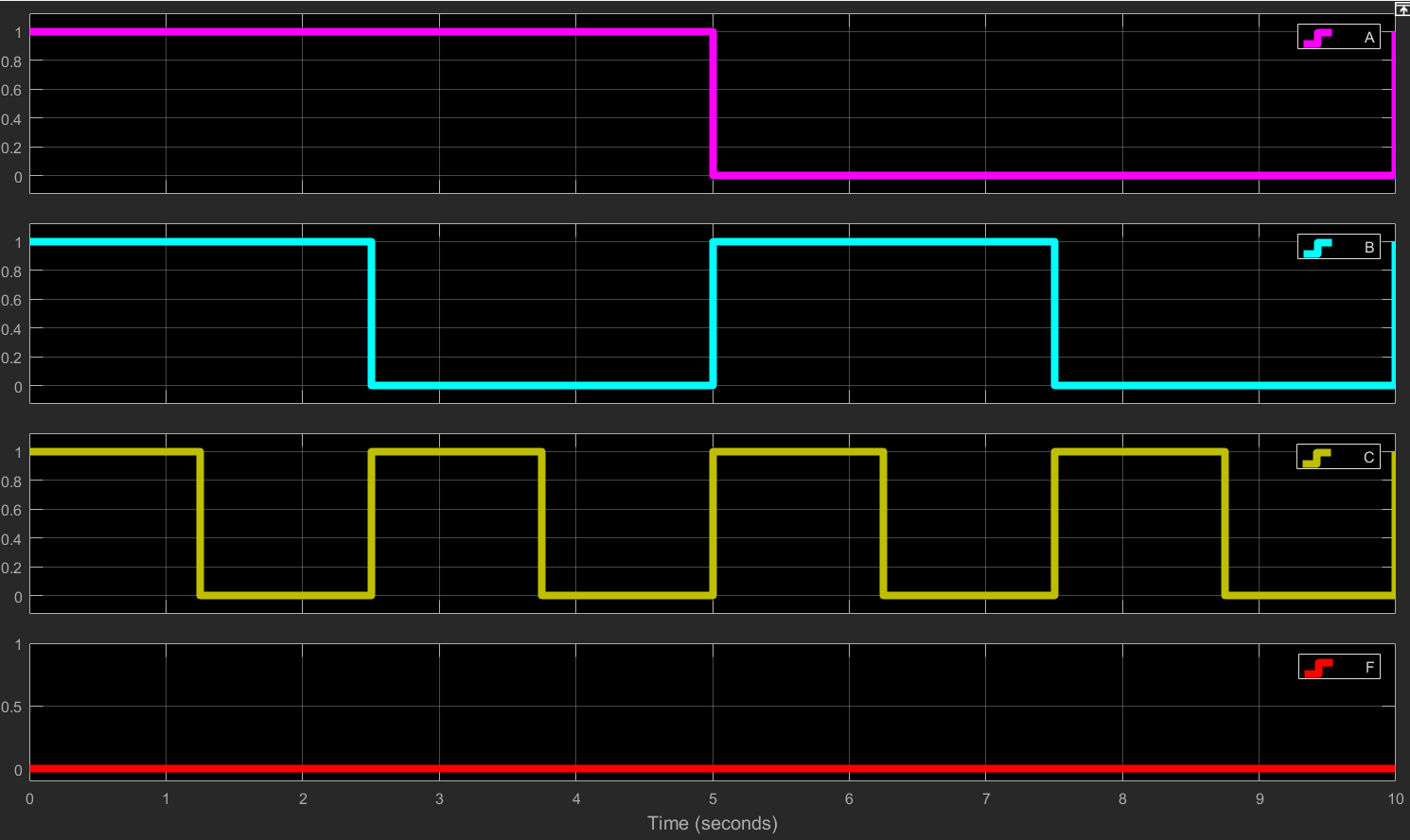




**Fig8i**: Simulink connections for circuit described as per statement in assignment part 2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | Output F | |
| Theoretical | Simulated |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 |

**Table8i**: Comparison between theoretical and simulated outputs of circuit in Fig

**Graphical Results:**

**Theoretical Results:**